IN THE SPECIFICATION:

Please amend the section title directly preceding paragraph number **[0001]**, together with paragraph number **[0001]**, as follows (and also by removing the underlining):

~~Related Applications~~ CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] This application is a continuation of pending U.S. App. Ser. No. 10/449,452 filed May 30, 2003, now U.S. Pat. No. 6,760,875, issued July 6, 2004; which is a continuation of U.S. App. Ser. ~~No. 10/155,398~~ No. 10/155,398 filed May 22, 2002 and issued as U.S. Pat. No. 6,591,386 on July 8, 2003; which is a continuation of U.S. App. Ser. No. 09/658,327 filed Sep. 8, 2000 and issued as U.S. Pat. No. 6,421,800 on July 16, 2002; which is a continuation of U.S. Application Ser. No. 09/324,738, filed Jun. 3, 1999 and issued as U.S. Pat. No. 6,138,258 on October 24, 2000; which is a divisional of U.S. Application Ser. No. 08/883,181, filed Jun. 26, 1997 and issued as U.S. Patent No. 5,944,845 on August 31, 1999.

Please amend the section title directly preceding paragraph number **[0002]** as follows (and also by removing the underlining):

~~Technical Field~~ TECHNICAL FIELD

Please amend the section title directly preceding paragraph number **[0003]** as follows (and also by removing the underlining):

~~Background of the Invention~~ BACKGROUND

Please amend the section title directly preceding paragraph number **[0006]** as follows (and also by removing the underlining):

~~Summary of the Invention~~ SUMMARY OF THE INVENTION

Please amend the section title directly preceding paragraph number **[0009]** as follows (and also by removing the underlining):

~~Brief Description of the Drawings~~BRIEF DESCRIPTION OF THE DRAWINGS

Please amend the section title directly preceding paragraph number **[0017]** (and also by removing the underlining), together with paragraph number **[0017]**, as follows:

~~Detailed Description of the Preferred Embodiments~~

DETAILED DESCRIPTION OF THE INVENTION

[0017] As FIG. 1 demonstrates, testing the operation of a memory circuit as taught by the prior art is generally performed by directing signals to a test vector decode circuit 10 from a plurality of memory addresses A_0 through ~~An,~~ A_n, wherein n is an integer. The test vector decode circuit 10 is usually a multiplexer, but regardless of the specific configuration of the test vector decode circuit 10, it will subject the inputs to one or more logic operations and generate a plurality of output test vectors V_0 through ~~Vm,~~ V_m, wherein m is an integer that may or may not be equal to integer n. In addition, a supervoltage detect circuit 12 is provided and is configured to respond to an external signal P by transmitting a supervoltage signal (SV) to a reset input terminal 14 of the test vector decode circuit 10.

Please amend paragraph number **[0018]** as follows:

[0018] The test vector decode circuit 10 resets all output test vectors V_0 through ~~Vm~~ V_m in response to a low SV signal. Thus, as long as SV remains at a high supervoltage potential, the output test vectors V_0 through ~~Vm~~ V_m maintain the values established as of the last logic operation. Logic operations are initiated by a signal sent to a latch input terminal 16 of the test vector decode circuit 10. In this embodiment, the test vector decode circuit 10 is configured to allow latching of the output test vectors V_0 through ~~Vm~~ V_m in response to a low WCBR signal, designated in FIG. 1 as WCBR*. This WCBR* signal is output by a WCBR detect circuit 18 which receives the signals RAS (Row Address Strobe), CAS (Column Address Strobe), and WE (Write Enable). FIG. 2 demonstrates the required state of these signals in order to latch the output test vectors: if (1) WE is low, and (2) CAS transmits a low signal before RAS does, then the WCBR circuit will output a WCBR* signal for latching the output test vectors V_0 through ~~Vm.~~ V_m. FIG. 2 also illustrates the cycle length of the test vectors in relation to the duration of the three signals. After the output test vectors V_0 through ~~Vm~~ V_m have been latched, they are used to drive external devices. Further inputs and latchings may be used to alter the drive of

these external devices. Once testing is over, however, the drive signals should generally maintain their value.

Please amend paragraph number **[0019]** as follows:

[0019] The combination of signals generating WCBR is chosen to trigger the latching of the output vectors because that combination is not intentionally used during ~~non-test~~ non-test operations of the memory device. This reduces the chance of accidental latching and changing of the output test vectors at inappropriate times. As mentioned above, however, that combination of signals may appear as a glitch in noisy environments such as the burn-in process.

Please amend paragraph number **[0026]** as follows:

[0026] One of ordinary skill can appreciate that, although specific embodiments of this invention ~~has~~ have been described for purposes of illustration, various modifications can be made without departing from the spirit and scope of the invention. For example, the memory device could be configured to provide a test vector lockout signal from an external device ~~22~~ 36 that is independent from the test vector decode circuit 10 and the output test vectors V_0 through ~~V_m,~~ V_m, as shown in FIG. 8. Furthermore, resetting the test vector lockout signal could also be independent from resetting all other output vectors. Such an embodiment could comprise sending a reset signal directly to the external device ~~22.~~ 36. Accordingly, the invention is not limited except as stated in the claims.